Digital Design

CSCE 2114-L007

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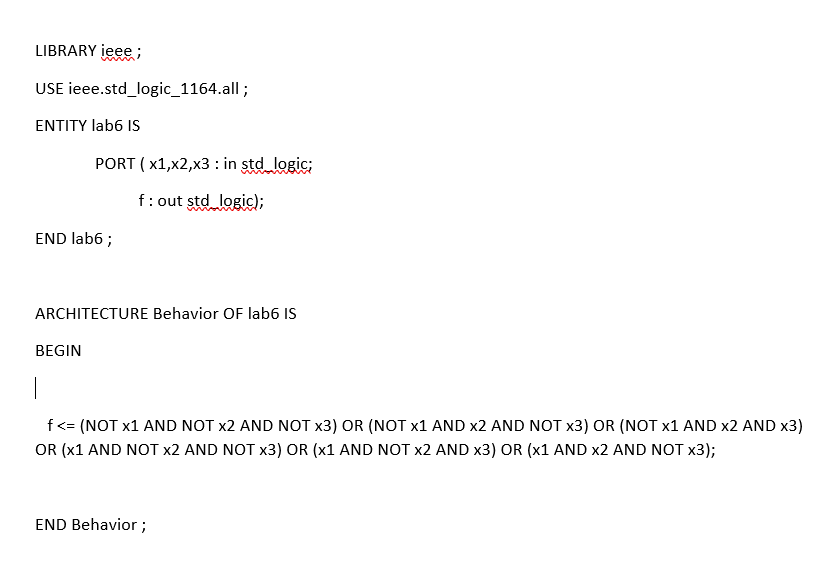
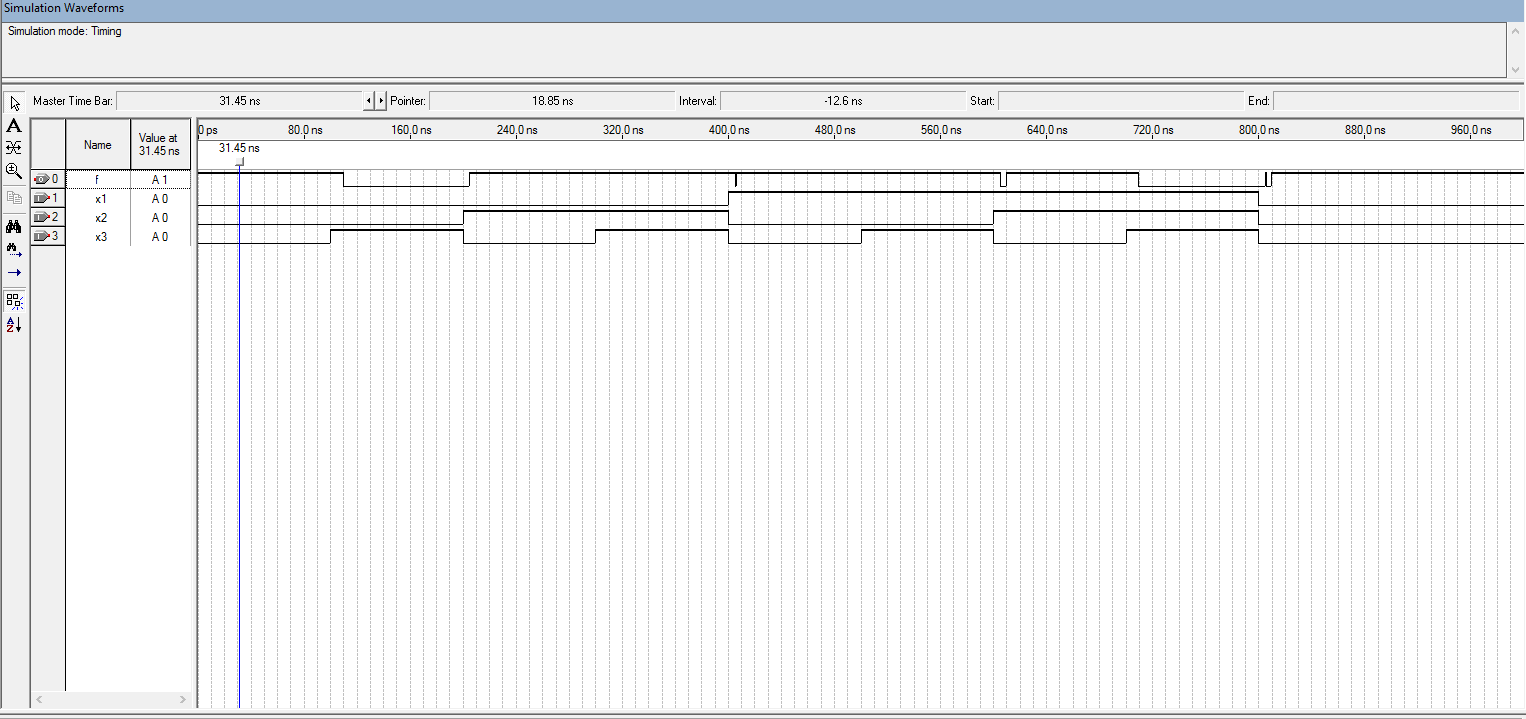
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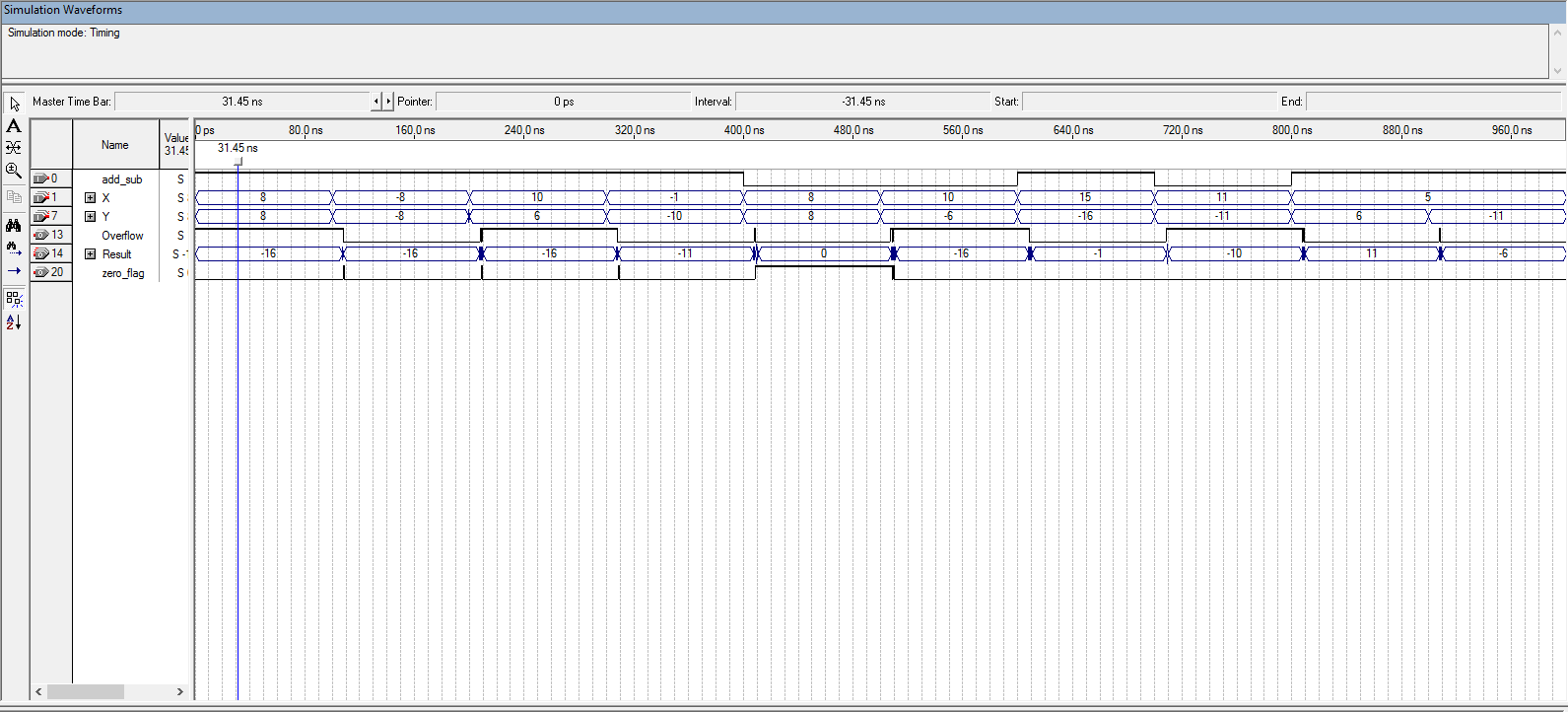
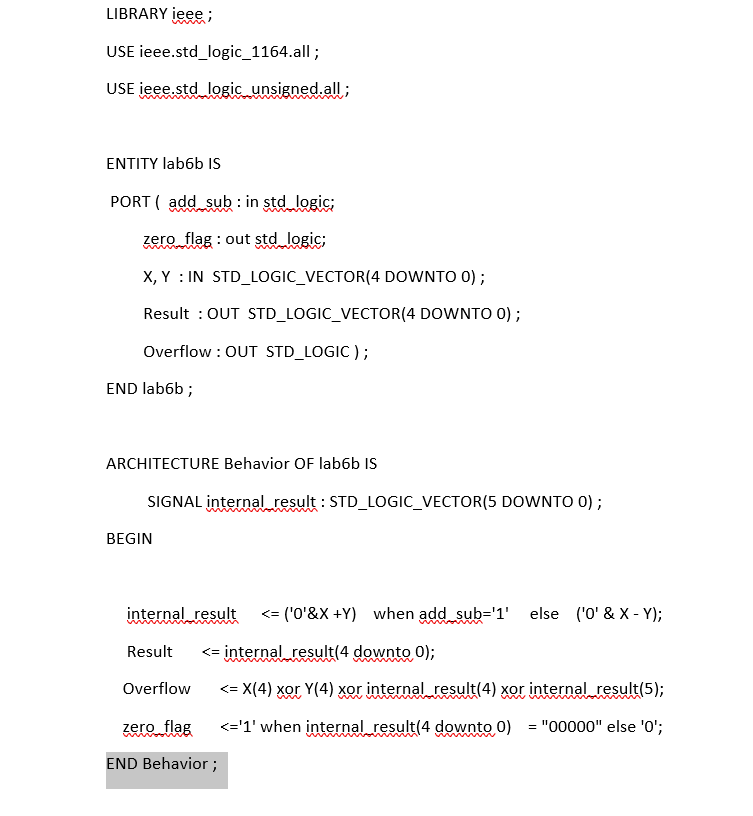
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**Introduction**

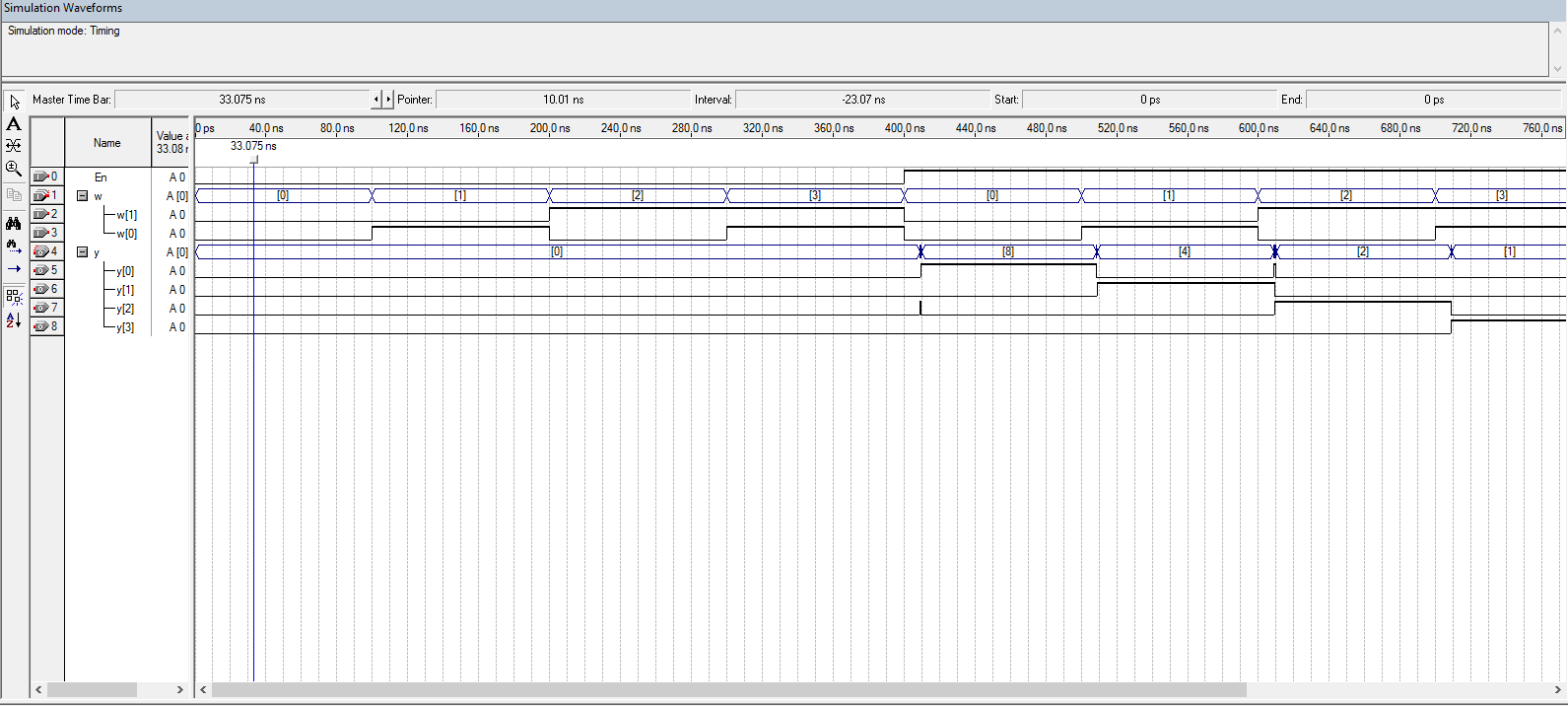
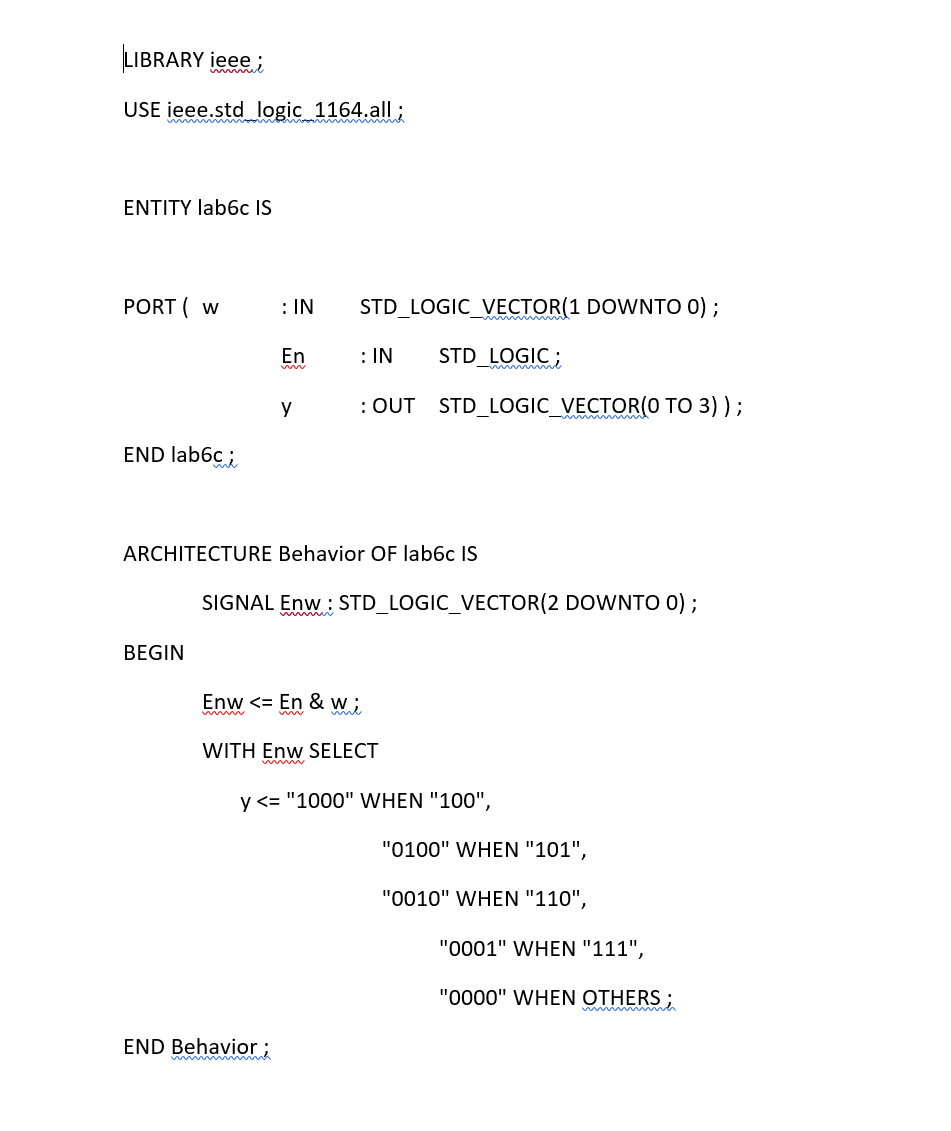
This lab is comprised of four sections split over two weeks. The purpose of this lab is write in VHDL code and to create simple circuits and also how to simulate the design in order to make sure that it works.

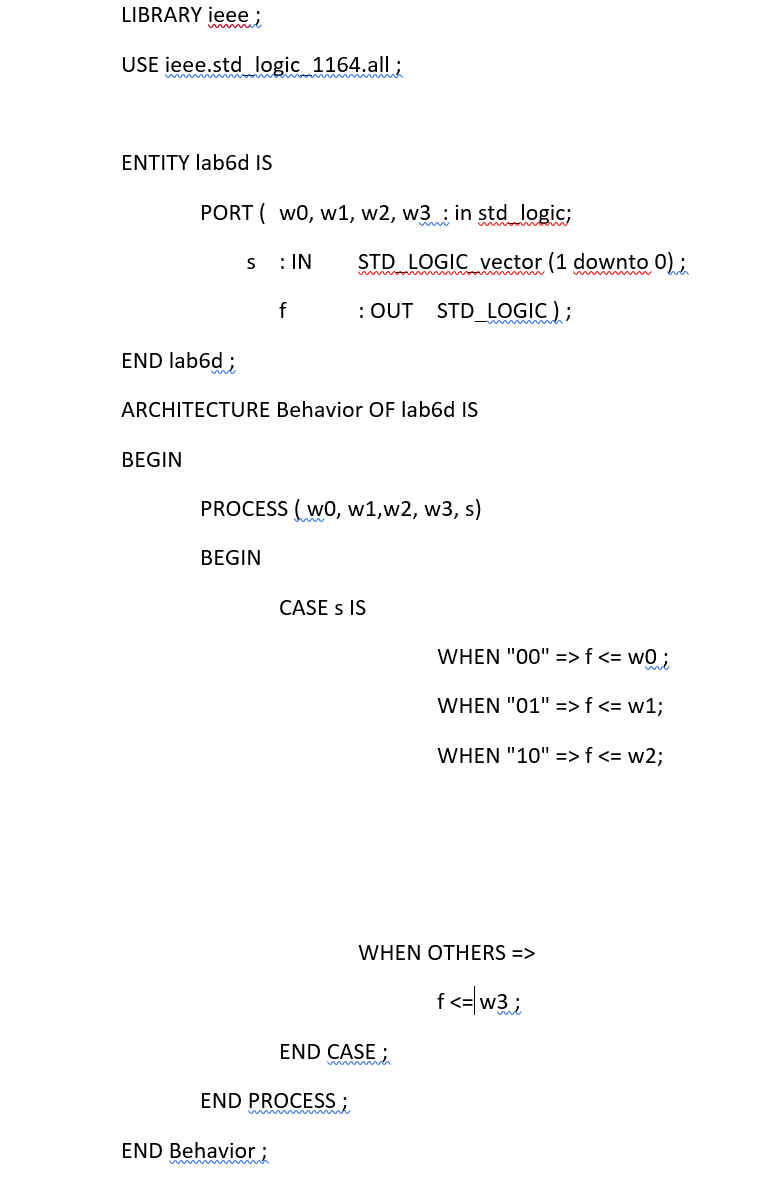
**Design**

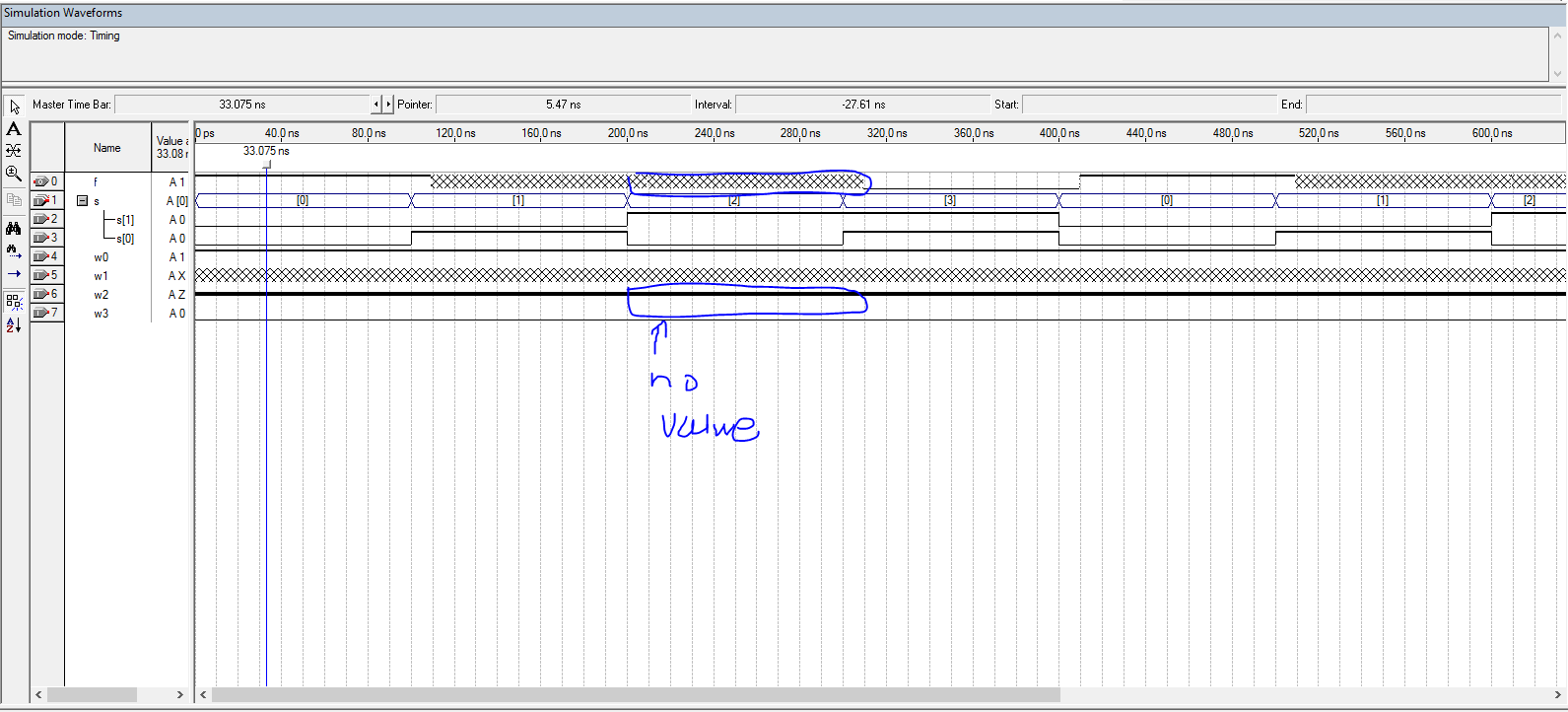
A lot of what was required in the VHDL code was very simple. In part A the function F(x1, x2, x3) = mΣ(0,2,3,4,5,6) was given and needed to be translated into VHDL code. The VHDL code for part A of this lab is shown below where the AND in front of each term means that term is a 1 and NOT means that the term is a 0. The simulation for part A will also be shown below.

Part B of the lab has three inputs and three outputs. Two of the outputs are X and Y and the third is an add\_sub. The outputs are the result of X and Y added or subtracted, an overflow detector, and a zero flag that detects when the answer is a 0. The range of the program is from –16 to 15. There were some cases to where the added values went beyond the range of the program and that is when overflow is detected, such as when the program added 8 and 8 together but the answer turned up –16 because overflow was detected. The only time the zero flag went up was when the program subtracted 8 and 8. The code for part B and the simulation are displayed below.

In part C the assignment said to make a decoder. The VHDL code has three inputs, w0, w1, and Enable, and four outputs, y0, y1, y2, and y3. All three inputs are either a 0 or a 1 and once w0 and w1 have cycled through Enable switches to a 1 and w0 and w1 cycles again. When Enable is 0 nothing happens to the output but once Enable switches to a 1, w0 and w1 start to have an effect on the output. Pictures of the VHDL code and the simulated output are shown below.



Implementing a 4 to 1 multiplexer in the goal of part D. The VHDL code has six inputs, w0, w1, w2, w3, s0, and s1, and one output. The input w0 is assigned to a value of 1, w1 is set to no value, w2 is set to high impedance, w3 is assigned a value of 0. Anytime that s0 and s1 are different values the output has no value. When both input values are set to 0 the output is a 1 and when both values are a 1 the output is a 0. The VHDL code and simulation are shown below.

**Conclusion**

This lab was meant to give a basic understanding of how to write and implement VHDL code. The lab has four sections that were split into two weeks with the first part of the lab taking longer to finish than the other.